

## METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

### BACKGROUND OF THE INVENTION

#### 5 Field of the Invention

**[0001]** This invention generally relates to a method for fabricating a semiconductor device, and more particularly to a method for fabricating a semiconductor device to enhance the uniformity of the semiconductor device.

#### Description of Related Art

10 **[0002]** As the line width and the size of the semiconductor device become smaller, it is unavoidable that the polysilicon electrode of the MOSFET and the memory device become smaller. When the integration of the devices increases, the resistance of the source region and the drain region usually increases. However, as the size of the device shrinks and its process margin declines, the uniformity of the semiconductor  
15 devices becomes worse.

**[0003]** During the fabrication of the MOSFET, after the gate electrode is formed by forming a gate oxide layer and a polysilicon layer, the spacer made of silicon oxide or silicon nitride will be formed on the two sidewalls of the gate electrode. Later on, the ion implantation is performed to form the source and drain regions at the two sides  
20 of the gate electrode and then the salicide process is performed. However, if the silicon oxide spacer is employed, a cleaning step has to be performed to remove the native oxide layer and impurity on the surface of the gate electrode and the substrate before performing the salicide process. A portion of the silicon oxide spacer may be removed during the cleaning step. Hence, the subsequently formed silicide would be

very close to the source/drain extension, which is easy to cause the junction leakage problems. On the other hand, if the silicon nitride spacer is employed to avoid the junction leakage problems, because the dielectric constant of silicon nitride is higher than that of silicon oxide, the silicon nitride spacer results in a larger parasitic

5 capacitance between the gate and the source/drain region, thus deteriorating the device performance.

[0004] A composite silicon oxide/silicon nitride spacer may also be formed on the sidewalls of the gate after defining the gate electrode. The composite spacer can be formed by forming an offset oxide layer covering the substrate and the gate electrode, 10 forming a silicon nitride layer covering the offset oxide layer and then performing anisotropic etching to remove a portion of silicon nitride layer until the offset oxide layer is exposed. The remaining offset oxide layer can protect the surface of the substrate when performing the ion implantation step to the substrate. However, when the size of the device and the line-width shrink, the thickness of each layer and the 15 process margin in each layer also become smaller. Especially, when the thickness of the offset oxide layer is less than or about  $100 \text{ \AA}$ , the thin offset oxide layer can easily be overetched and the thickness of the remaining offset oxide layer is not uniform in various locations. Since the thickness of the remaining offset oxide layer is varied, the junction depth of the source/drain region becomes non-uniform after the ion 20 implantation step through the non-uniform offset oxide layer. In addition to the non-uniform depth of the source/drain region, the effective channel length of the gate electrode may be changed, which significantly affects the uniformity of the semiconductor devices on the wafer.

## SUMMARY OF THE INVENTION

**[0005]** An object of the present invention is to provide a method for fabricating semiconductor device in order to prevent junction leakage, reduce the parasitic capacitance between the gate and source/drain regions, and enhance the uniformity of the semiconductor devices.

**[0006]** The present invention provides a method for fabricating a semiconductor device, comprising: providing a substrate; forming a gate structure on the substrate, the gate structure including a gate dielectric layer on the substrate and a gate conductive layer on the gate dielectric layer; forming an oxide layer conformally covering the substrate and the gate structure; forming a dielectric layer covering the oxide layer; removing a portion of the dielectric layer to expose the oxide layer and to form a spacer on a sidewall of the gate structure, the oxide layer between the spacer and the gate structure as an oxide spacer; performing an oxygen plasma treatment process to form an silicon oxide layer in the substrate below the exposed oxide layer using the gate structure and the spacer as masks, the silicon oxide layer and the oxide layer constituting an uniform offset oxide layer; and forming a source/drain region in the substrate at two sides of the gate structure. The method of this invention can further comprises performing a cleaning process to clean the surface of the substrate and forming a silicide layer on the source/drain region.

**[0007]** The present invention provides a semiconductor device, at least comprising: a substrate; a gate structure on the substrate, the gate structure including a gate dielectric layer on the substrate and a gate conductive layer on the gate dielectric layer; an oxide spacer on a sidewall of the gate structure; a spacer on the oxide spacer; a source/drain region in the substrate besides the gate structure and the spacer; and an

offset oxide layer covering the substrate and the source/drain region, the offset oxide layer having a bottom surface below a bottom surface of the gate dielectric layer.

[0008] Because in the present invention an oxygen plasma treatment process is performed before performing the source/drain ion implantation step in order to form an  
5 uniform offset oxide layer on the substrate, the depth of the subsequently formed source/drain regions will be uniform, which provides a constant effective channel width.

[0009] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description,  
10 accompanying drawings and appended claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGs. 1A-1F show the cross-sectional view of the process for fabricating a semiconductor device in accordance with a preferred embodiment of the present  
15 invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0011] FIGs. 1A-1F show the cross-sectional view of the process for fabricating a semiconductor device in accordance with a preferred embodiment of the present  
20 invention.

[0012] Referring to FIG. 1A, a substrate 100 such as a silicon substrate is provided. The substrate 100 includes an isolation structure 101 such as LOCOS or STI, and other semiconductor devices. A gate dielectric layer 102 is formed on the substrate 100. A gate conductive layer 104 is formed on the gate dielectric layer 102.

The gate dielectric layer 102 is, for example, an oxide layer. The gate conductive layer 104 can be doped polysilicon formed by in-situ doping by CVD, for example.

[0013] Referring to FIG. 1B, a gate structure 106 is formed by defining the gate dielectric layer 102 and the gate conductive layer 104 using photolithographic and  
5 etching technology.

[0014] Then an ion implantation process 108 is performed by using the gate structure 106 as a mask to form the lightly doped source/drain extension region 110 in the substrate 100 at the two sides of the gate structure 106.

[0015] Referring to FIG. 1C, a conformal oxide layer is formed on the substrate  
10 100 to cover the gate structure 106 and the substrate 100. The oxide layer 112 can be silicon oxide formed by CVD and using tetra ethyl ortho silicate (TEOS)/ozone, for example. The thickness of the oxide layer 112 is about 50-300 Å, for example. Then a conformal dielectric layer 114 is formed on the oxide layer 112 to cover the substrate 100 and the gate structure 106. The dielectric layer 114 has a high etching selectivity  
15 related to the oxide layer, and the dielectric layer 114 will not be affected when removing the native oxide layer. The dielectric layer 114, for example, is made of silicon nitride by CVD. The thickness of the dielectric layer is usually larger than that of the oxide layer.

[0016] Referring to FIG. 1D, a portion of the dielectric layer 114 is removed  
20 until the oxide layer 112 is exposed. Only the dielectric layer 114 on the sidewall of the gate structure is remaining as the spacer 120. The oxide layer between the spacer 120 and the gate structure 106 can be deemed as an offset oxide spacer 118. The thickness of the offset oxide spacer 118, e.g., 50-200 Å, is smaller than that of the spacer 120. The portion of the dielectric layer 114 can be removed by anisotropic

etching such as reactive ion etching (RIE). Taking advantage of the high etching selectivity of the oxide layer to the dielectric layer, the dielectric layer 114 is removed until the oxide layer 112 is exposed. After removing the dielectric layer 114 and forming the spacer 120, the oxide layer 112 is exposed except the oxide layer below the spacer 120 is covered the spacer 120.

[0017] Because the remaining oxide layer 112 on the substrate can protect the surface of the substrate from damage due to the subsequent ion implantation, if the remaining oxide layer is non-uniform at the source/drain region, the depth of the source/drain region becomes non-uniform after the ion implantation. Referring to FIG. 1E, to improve the uniformity of the oxide layer, especially the oxide layer covering the subsequently formed source/drain region, an oxygen plasma treatment process is performed by using the spacer 120 and the gate structure 106 as masks. A gas source including oxygen is flowed into the chamber to generate the plasma and the DC power of 100-2000W is applied, for example. With the plasma treatment process, oxygen atoms are implanted to the surface of the substrate, especially the substrate predetermined for forming source/drain region, and reacted with the substrate to form silicon oxide. That is, a thin oxide layer will be formed below the oxide layer 112 so that an offset oxide layer 124 with a uniform thickness is formed. The applied DC power, the implantation dosage and the treatment time can be adjusted based on the required thickness of the offset oxide layer.

[0018] Because the oxygen plasma treatment process is performed by using the spacer 120 and the gate structure 106 as masks, the implanted oxygen atoms only react with the exposed oxide layer. The implanted oxygen atoms will only react with the silicon atoms of the substrate (consuming the silicon atoms of the substrate) to form the

silicon oxide. Further, the thickness of the remaining oxide layer covering the substrate will affect the depth and the density of the implanted oxygen atoms, because the plasma treatment process is performed through the oxide layer covering the substrate. That is, the thicker the remaining oxide layer is, the lesser silicon oxide is later formed, and vices versa. Hence, the later formed silicon oxide can counterbalance (offset) the non-uniformity of the remaining oxide layer and forms a uniform offset oxide layer 124. The offset oxide layer 124 includes the remaining oxide layer 112 and the silicon oxide formed by the oxygen plasma treatment process.

[0019] The implanted oxygen atoms will also be implanted into the gate conductive layer of the gate structure through the oxide layer 112 covering the top surface of the gate structure 106. If the material of the gate conductive layer is polysilicon, the implanted oxygen atoms will react with the polysilicon to form silicon oxide so that the oxide layer 112 on the gate structure 106 will become thicker. However, because the depth of the implanted oxygen atoms is not too deep, it will not consume too much silicon in the polysilicon layer and the performance of the gate structure will not be seriously affected.

[0020] Referring to FIG. 1F, an ion implantation process 126 is performed by using the spacer 120 and the gate structure 106 as masks to form the heavily doped source/drain region 128 in the substrate 100 at the two sides of the spacer 120 and the gate structure 106. Because there is a uniform offset oxide layer 124 on the substrate, the depth of the source/drain region 128 is uniform and the effective channel length is unvaried.

[0021] Later, if necessary, a self-align silicide process can be performed depending on the types of the devices. Because the self-align silicide process is well

known by the one skilled in the art, no detailed description is necessary. Before self-align silicide process, an additional cleaning process is required to remove the oxide layer and the impurity between the gate and the surface of the substrate. The aforementioned offset oxide layer will also be removed.

5   **[0022]**        In the above embodiment, the oxide layer can be silicon oxide or a dielectric material with a dielectric constant less than 4 to reduce the parasitic capacitance and enhance the performance of the device. The material of the dielectric layer can be silicon nitride, SiON, or other material having a high selectivity related to the oxide layer.

10   **[0023]**        The semiconductor device based on the above embodiment as shown in FIG. 1F comprises: a substrate 100; a gate structure 106 on the substrate 100, the gate structure 106 including a gate dielectric layer 102 on the substrate 100 and a gate conductive layer 104 on the gate dielectric layer 102; an oxide spacer 118 on a sidewall of the gate structure 106; a silicon nitride spacer 120 on the oxide spacer 118; a  
15   source/drain region 128 in the substrate 100 besides the spacer 120 and the gate structure 106; and an offset oxide layer 124 covering the substrate 100 and the source/drain region 128, the offset oxide layer 124 having a bottom surface below a bottom surface of the gate dielectric layer 102. It further comprises a source/drain extension region below the oxide spacer 118.

20   **[0024]**        Because a uniform offset oxide layer 124 is formed on the substrate by performing the oxygen plasma treatment process, the depth of the source/drain region 128 is uniform so that the effective channel length will not be affected and the uniformity and performance of the device will be enhanced.

**[0025]**        The above description provides a full and complete description of the



preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is

5 defined by the following claims.